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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Hronik, Stanley A.		
Assignee:	Integrated Device Technology, Inc.		
Title:	DOUBLE DATA RATE SYNCHRONOUS SRAM WITH 100% BUS UTILIZATION		
Serial No.:	09/347,106	Filed:	July 2, 1999
Examiner:	Anderson, Matthew D.	Group Art Unit:	2186
Docket No.:	M-7086 US		

San Jose, California
May 21, 2002

COMMISSIONER FOR PATENTS
Washington, D. C. 20231

PRELIMINARY AMENDMENT AND ELECTION OF CLAIMS

Sir:

This is a reply to the Office Action mailed April 22, 2002, please amend the above-identified application as follows (a version with markings to show changes made appears at the end):

IN THE SPECIFICATION

Please amend the paragraph on page 1, line 25, through page 2, line 4, to read as follows:

The input and output registers however, cause two clock cycles of latency in the relation between the read address and read data, and no latency between the write address and write data (i.e., the address is clocked in and the data is clocked out in two consecutive clock cycles for a read, and the address and data are clocked in in the same clock cycle for a write). This latency difference between read and write operations causes the address bus to remain idle for two clock cycles when a read cycle is followed by a write cycle, and causes the data bus to remain idle for two clock cycles when a write cycle is followed by a read cycle (i.e., bus turnaround). The idle cycles reduce the system data bandwidth.

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